

A113X I2S Input Timing and Power Sequence Test Report of Audio Abnormal Sample for Pre-MP Build

1. I2S Timing Specification

Figure 18 I2S/TDM Timing Diagram, Slave Mode

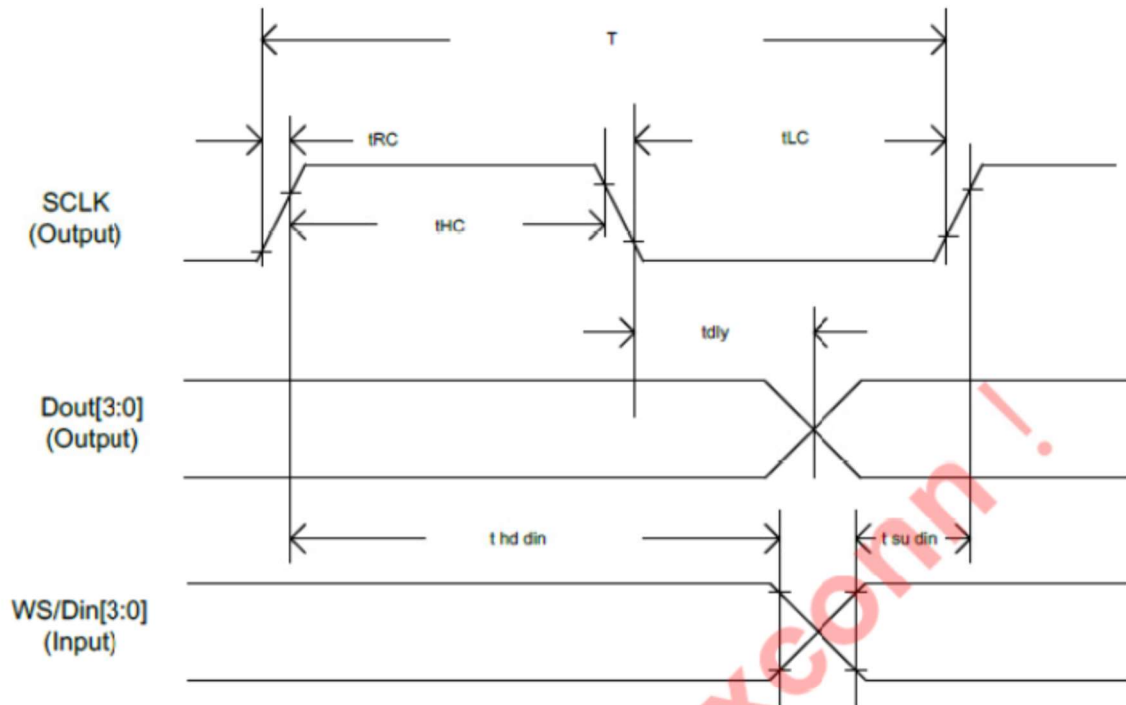


Table 34 Audio I2S/TDM Timing Specification, Transmitter, Slave Mode

Transmitter (slave mode)					
Symbol	Parameter	Min	Typ	Max	unit
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/Din	4			ns
tdly	Delay between SCLK and Dout	2	7	10	ns

2. I2S Timing Test Result and Picture

	Parameter	Symbol	Min	Max	Unit	Result	Pass /Fail	Figure
A113X Input Timinf	Clock period	T(in)	10		ns	326.133	Pass	1
	High level of SCLK	tHC	0.4		T	0.45	Pass	2
	Low level of SCLK	tLC	0.4		T	0.47	Pass	3
	Edge time of SCLK	tRC		26	ns	12.632	Pass	4
	Setup time of WS	Tsu in	4		ns	161.03	Pass	5
	Setup time of Din	Tsu in	4		ns	181.224	Pass	6
	Hold time of WS	Thd in	4		ns	150.927	Pass	7
	Hold time of Din	Thd in	4		ns	145.835	Pass	8

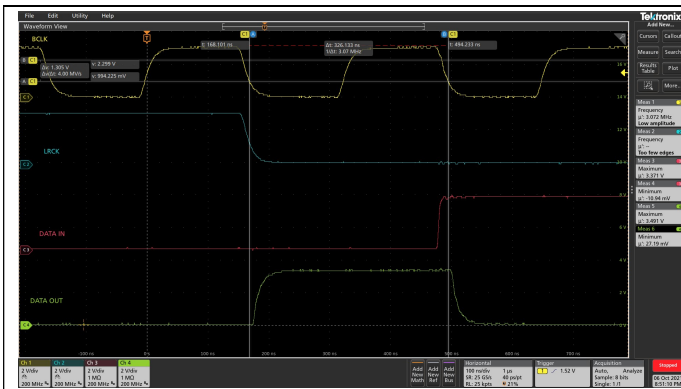


Figure 1: Clock period

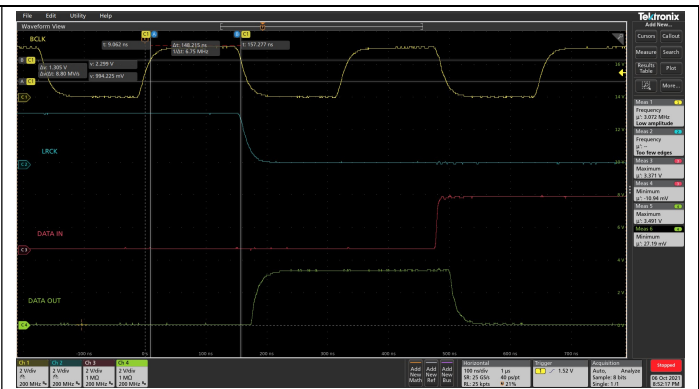


Figure 2: High level of SCLK

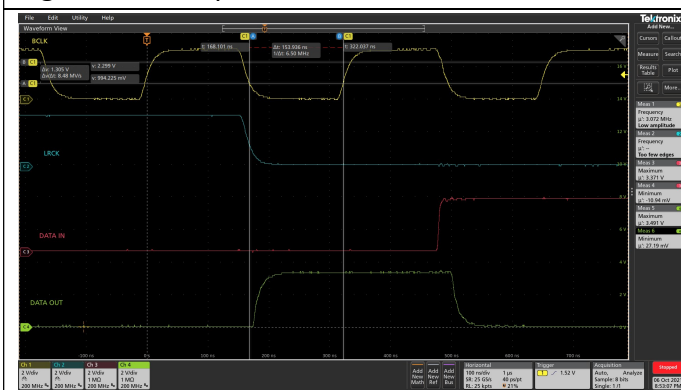


Figure 3: Low level of SCLK

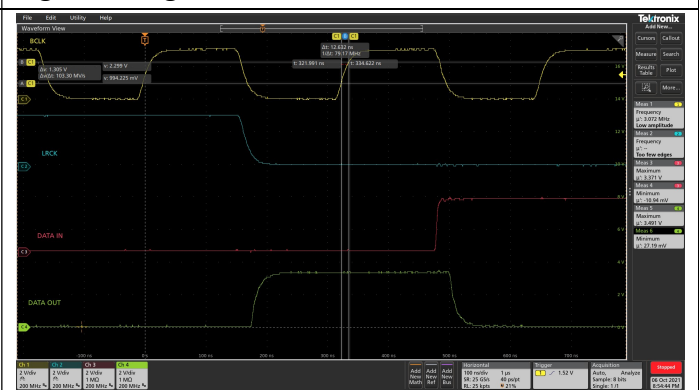


Figure 4: Edge time of SCLK

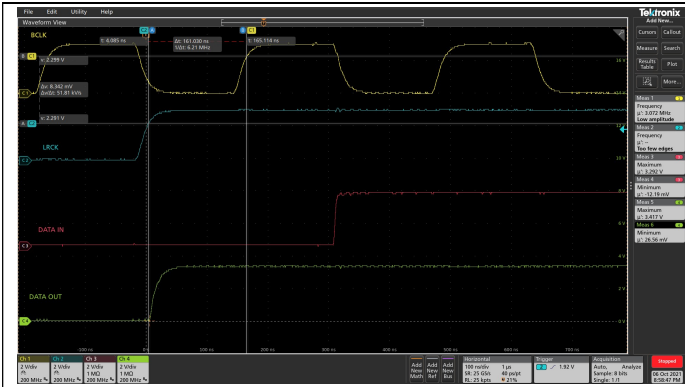


Figure 5: Setup time of WS

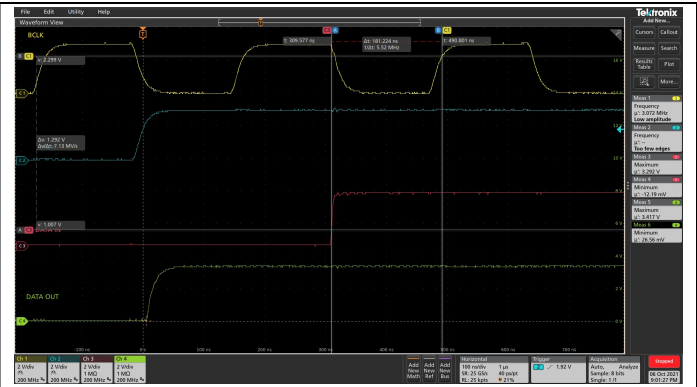


Figure 6: Setup time of Din

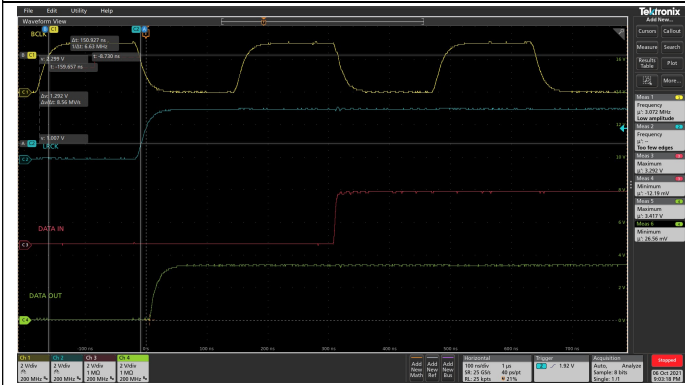


Figure 7: Hold time of WS

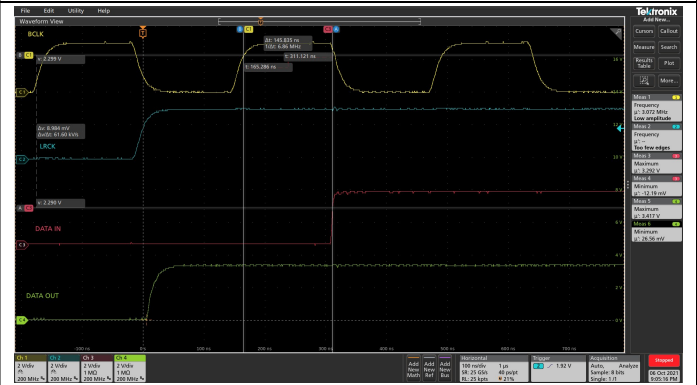


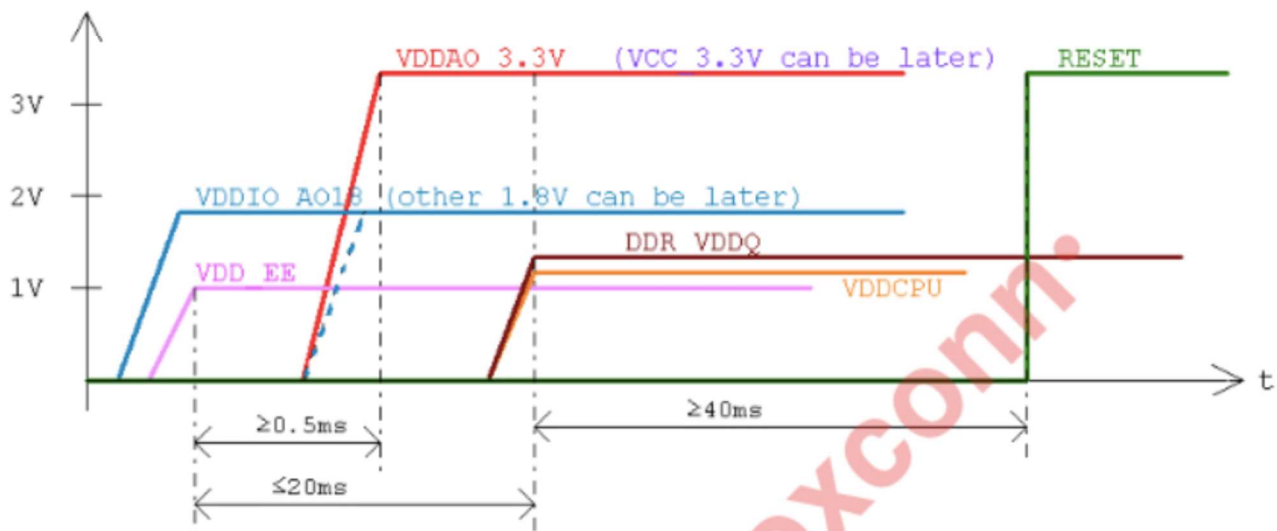
Figure 8: Hold time of Din

3. Power Sequence Specification

4.9 Recommended Power on sequence

Example power on sequence:

VDD_EE -> VDDIO_AO3.3V& VDDIO_AO18 -> VCC3.3V&VDDIO1.8V&AVDD1.8V -> VDDCPU&DDR_VDDQ



Note:

- 1) VDDIO_AO3.3V&VCC3.3V should ramp up $> 0.5\text{ms}$ later than VDD_EE
- 2) All power sources should get stable within 20ms(except for DDR_VDDQ)
- 3) No sequence requirement between IOVREF_18 and VDD_EE
No sequence requirement between VDDCPU & DDR_VDDQ and other power source
- 4) IOVREF (VDDIO_AO18) should ramps up earlier or at the same time with VDDIO_AO3.3V & VCC3.3V, VDDIO_AO3.3V & VCC3.3V should never be 2.5V higher than IOVREF_18.
- 5) In some designs, VDDCPU & VDD_EE are merged to VCC_CORE, the power on sequence should be same as VDD_EE.
- 6) RESET_n should keep low for at least 40ms after power up(except DDR_VDDQ)

Please refer to reference schematics.

4. Power Sequence Test Result and Picture

Test Item	Test Result (ms)	Figure	Spec. (ms)	Pass/Fail
VDD_EE vs VDDAO_3.3V	1.568	9	≥ 0.5	Pass
VDD_EE vs VDDCPU	4.537	10	≤ 20	Pass
VDD_EE vs VDDQ1.35V	1.934	11	≤ 20	Pass
VDD_EE vs VDDIO_AO18	0.155	12	TBD	Pass

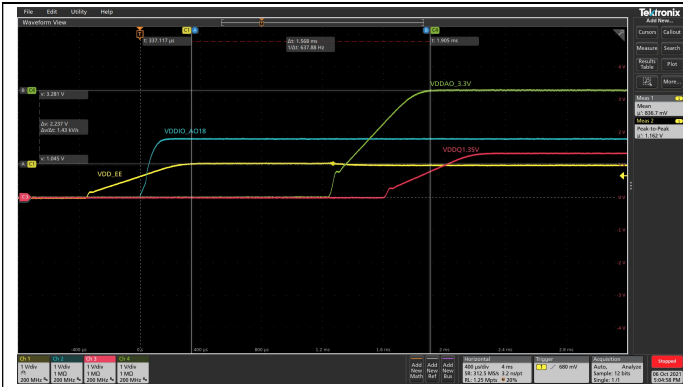


Figure 9: VDD_EE vs VDDAO_3.3V

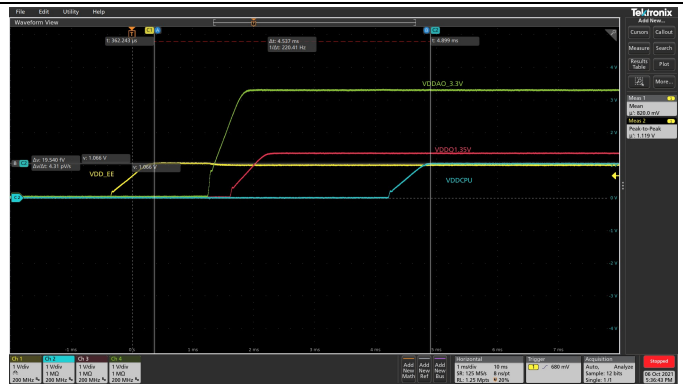


Figure 10: VDD_EE vs VDDCPU

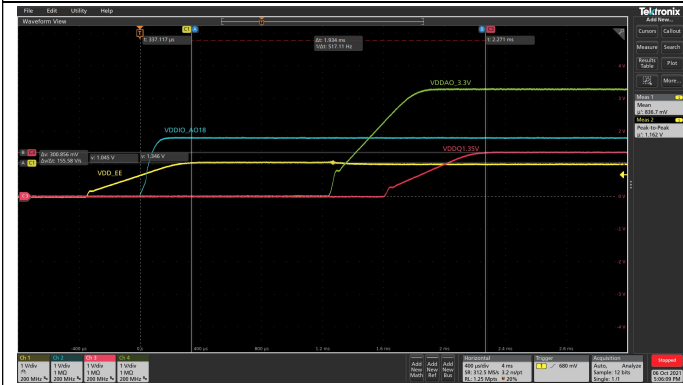


Figure 11: VDD_EE vs VDDQ1.35V

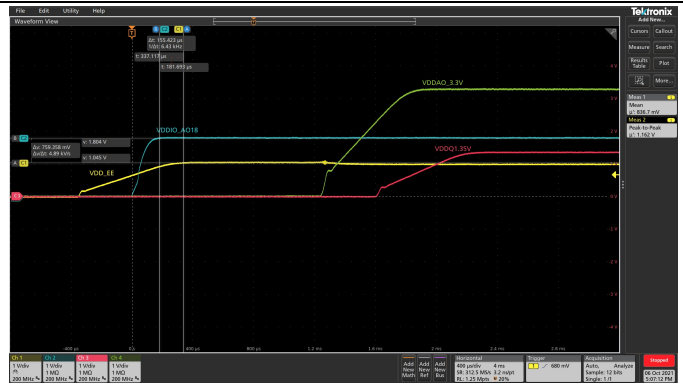


Figure 12: VDD_EE vs VDDIO_A018